



Turnkey ASIC solutions – The one-stop shop approach

The DELTA team, located in Denmark and the UK, provides the complete mix of design and industrialisation services needed to successfully bring your new or existing product into an ASIC technology and so realise decreased cost combined with increased performance and quality

Introduction

DELTA has 20+ years experience in providing a complete set of services for development and industrialisation of ASICs. Our services range from feasibility analysis of your product / business case to specification, architectural design / behavioural modelling, detailed design in analog and digital domains, mixed signal verification, layout and conversion to silicon for prototype verification and volume production setup. In addition, DELTA offers small to medium volume delivery of components / dies – and if that is not enough we can offer to help you to transfer production to the Far East for lower cost at high volume.

The reuse methodology

A key parameter in the success of our approach is that it is based on the reuse of selected sets of functional blocks, each verified in silicon/FPGA, that can be reassembled in your customised configuration. This significantly reduces risk and cost, and shortens time to market. DELTA is continuously expanding its portfolio of IP in key application areas.

Excerpts from the catalogue:

- 8/32 bit processor cores
- UART, IIC Core, USB 1.1
- LVDS I/Os
- DES/3DESS processor
- SHA-1 hash
- HDLC controller (DSRC)
- ADCs 8 – 10 bit, DACs 8 – 10 bit
- 16 Bit Sigma Delta ADC
- Bandgap vref.
- Op. amplifiers, instrumentation amplifiers, transconductance amplifiers, Switched CAP amplifiers

- PLLS (32 kHz – 16 MHz)
- Voltage reg., ULP Voltage Reg.
- RC osc. ULP, X-Osc ULP, POR and Brown Out Detectors
- Photodiode sensor based on standard CMOS Process
- Hall effect sensors
- DSRC analog front-end & baseband
- RFID 14443/15693 analog front-ends
- RFID 14443 / 15693 modulator / demodulator
- EPC GEN2 front-end (UHF RFID) (in development)
- EPC Gen 2 modulator/demodulator

The phased development approach

Our design methodology is based on a phased approach, where we, for each phase hold a gate review with you including a risk assessment revised throughout the project. Our flexibility allows a variety of entry points into the phased model, depending on your capabilities.

A typical entry point is a feasibility phase, with (preliminary) requirements spec, VHDL / Verilog code hand-off or RTL hand-off. A project manager will be assigned to carry your project from start to volume production hand-over.

Feasibility and specification

- Feasibility analysis of customer requirement spec.
- Update / approval of requirement spec.
- Choice of technology
- Availability of IP
- ASIC architecture proposal
- Risk assessment
- Development plan for the complete project
- Commercial proposal for design and component delivery



Analog / mixed signal design

- Ultra low power / low voltage analog / mixed signal design
- Block level simulation, post layout simulation, modelling (Verilog A)
- Sub-threshold design (weak inversion)
- Chip architecture (power supplies, Power On Reset, pads, floorplan, power distribution, substrate)
- Design / layout for low noise considerations
- Test harness design
- Layout at block and chip level
- LVS & DRC

Digital design

- Digital IC design and verification
- RTL coding (VHDL, Verilog)
- Synthesis
- System integration of 3rd party
- IP's, ROM, RAM, EEPROM, OTP
- DFT methodology (JTAG, BIST, Scan Insertion)
- Clock tree insertion
- Floorplanning (power distribution, IR-drop)
- Place&Route
- Static Timing Analysis
- LVS & DRC

Verification / Test

- Mixed signal verification at chip level (VHDL/Verilog, RTL, Verilog-AMS, Spice)
- Scripted simulations for regression testing
- Scripted corner / Monte Carlo simulations
- Equivalence checking
- ATPG, production test vector generation
- Test program development for production testing
- Failure analysis capabilities in-house ita

Delivery of components

- Prototype assembly in-house
- Packaging of components
- Qualification testing (HTOL, ESD, Burn-in)
- Volume production testing in-house (packaged or at wafer level)
- Yield analysis and optimisation

DELTA

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NanoComplete

DELTA can, in cooperation with our partner, Sondrel, offer total solutions for SoC type designs in deep submicron processes targeting the complex and high speed SoC application area.

Technologies

- CMOS 0.8 μ to 0.18 μ and beyond
- BICMOS

Tools

- CADENCE (Analog, Digital, Mixed Signal and Encounter P&R)
- MatLab incl. Simulink
- Modelsim
- Synopsys synthesis
- Mentor Graphics DftAdvisor, FastScan and FlexTest
- Calibre LVS&DRC
- Verigy 93000 RF and high pin-count testers (2 pcs.)
- Verigy 83000 digital tester
- Teradyne Catalyst mixed signal tester
- Teradyne A585 mixed signal tester
- Teradyne J750 digital tester
- X-Ray, SEM and more for failure analysis. Access to FIB
- Wire bonding and flip chip for prototype assembly

Key application areas

- DSRC Tollroad transponders
- RFID tags for niche applications (privacy functions, connected health applications, sensor interfaces etc.)
- Ultra low power / low voltage battery operated sensor interface devices
- Optical sensor applications
- Retarget of (standard) components to ASICs

How to get started

DELTA offers a very flexible approach to the entry point. We split the development responsibility in line with your needs. If you already have a prototype we can start by analysing your business case and calculate the possible cost savings and product performance improvements.

For further information please contact

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