

Single channel HDLC controller core

Features

- Fully synchronous design, clocked on rising clock edges
- Asynchronous reset
- Fully registered, synchronous interfaces
- Full duplex transmission/reception
- Frame checking sequence in hardware (CRC-16)
- Hardware recognized/added flag pattern '01111110'
- Simple CPU interface:
- Separate 8-bit data buses for data input and output
- 4-bit address bus
- Single chip select
- Single read/write signal
- User selectable configurations:
 - Transmitter only
 - Receiver only
- Individual data encoding/decoding: NRZ or NRZI
- Transmitter preamble of 9 '1's and 8 '0's
- Transmitter postamble of 8 '1's
- Transmitter interrupt after end flag
- Receiver interrupt after end flag
- Indication of Transmitter FIFO underrun
- Indication of Receiver FIFO overrun
- Address filter:
 - 1 or 4 bytes private address filtering
 - 1 user selectable broadcast address
 - Approx 5000 gates in 0.35 μ @ 50 MHz

Deliverables

- Fully synthesizable VHDL-RTL source code
- Test bench
- User documentation
- Synopsys synthesis script

Introduction

The Single Channel HDLC Controller Core developed by DELTA is a basic HDLC core that is easily implemented in any system. It is a high performance core module for bit-oriented data transmission.

It contains a 16-bit frame checking sequence (FCS), flag insertion/ detection, zero insertion/deletion, and abort generation/ detection. It is designed with advanced features such as transmitter/receiver FIFOs, address field recognition, and frame length count. The core has a CPU interface which easily can be adapted for a wide range of microprocessor interfaces. The CPU Figure 1: Frame Format controls the HDLC controller through registers inside the HDLC controller. These registers are described in section 9.

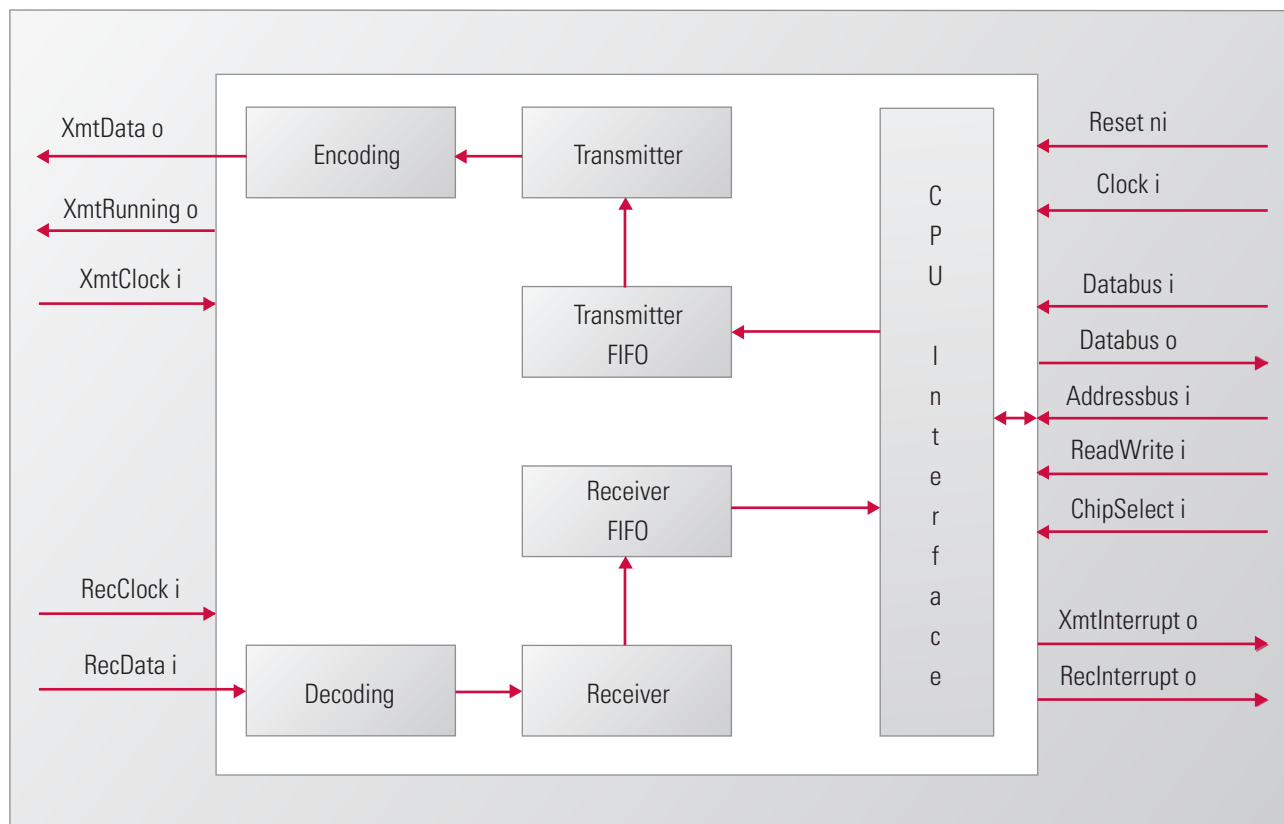
The core can be configured to contain either a receiver or transmitter or both. The controller includes two types of encoding/decoding which is individually configurable for the receiver and transmitter. The types are NRZ and NRZI coding. Clock generation and clock recovery is kept outside the scope of the HDLC core.

The frame format is shown in below. The transmitter is transmitting the pre- and postambles as specified, and the receiver is ignoring the pre- and postamble fields.

```
Preamble: 9 '1' + 9 '0'
Start flag: 0x7e
Address: 1-4 octets
Data: 0-124 octet
FCS: 2 octets
End flag: 0x7e
Postamble: 8 '1'
```

Frame Format

Figure 1: HDLC controller core



For further information please contact

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